REMARKS

The above application has been amended and reconsideration and re-examination are requested.

The Examiner objected to claims 3-6, 13, 15, 23, 30 and 33. Applicants have changed the term "selectivity" to the term "sensitivity" in claims 4, 13, and 23. Additionally, Applicants have modified claims 30 and 33 to depend on claim 1.

In addition, Claim 3 has been amended to clarify that the computer instruction is imported from memory, claim 5 has been amended to clarify that the computer instruction is used for capturing data, and claim 6 has been amended to clarify that the set of abstractions represent hierarchical levels of the logic design. Claim 15 has been amended to correct a typo. Accordingly, withdrawal of the claim objections is respectfully requested.

The Examiner rejected claims 1-6, 11-16, 21-26, and 31-33 under 35 U.S.C. 102(b) as being anticipated by Sharma et al. (US 5,491, 640). Claims 7, 8, 10, 17, 18, 20, 27, 28, and 30 were rejected as being obvious over Sharma in view of the Jain Paper entitled A Comprehensive Pre-RTL IC Design Methodology.

Applicants' claims are distinct over the references. Sharma neither describes nor suggests embedding a computer instruction within a two-dimensional schematic representation, wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD), as recited in claim 1 for instance. Furthermore, Sharma neither discloses nor suggests the computer instruction being devoid of declarations as also recited in claim 1.

Sharma is directed towards optimally synthesizing an IC HDL specification by including both combinational and sequential components in a datapath library and by mapping HDL specifications implying sequential logic to sequential components, rather than to combinational components (col. 7, lines 58 to 61). Sharma's method involves decomposing an HDL description of a circuit, such as that shown in Sharma FIG. 4, into data flowcharts to delineate the portions of the HDL description that would be implemented with sequential logic from the portions that are implemented using combinational logic. Examples of such flowcharts used by

Sharma are CDFGs (col. 5, lines 56-66) and expression trees described in FIG. 5a-5b and accompanying text in col. 7, lines 7 – 40.

By contrast, Applicants' claim1 is directed toward embedding a computer instruction, (e.g., a textual design such as an HDL description) within a two-dimensional schematic representation of a design. As described in Applicants' specification on pages 5 and 7, embedding the HDL within a schematic representation mitigates ambiguities that can occur when the designer makes changes to the HDL, but forgets to update the changes in the schematic and vice versa. Embedding a computer instruction within a schematic representation enables the schematic representation to be automatically updated when the HDL changes; and likewise, the HDL to be automatically updated when the schematic changes.

On page 3, part 5 of the Office Action, Examiner incorrectly equates Sharma's CDFGs and expression trees to Applicants' two-dimensional schematic representation. Claims 1, 11, and 21 recite that the two-dimensional schematic representation includes a set of register transfer diagrams (RTD). An RTD is described in Applicants' specification on page 3 as being "a hierarchical diagram that contains all state elements and combinatorial logic that can be abstracted at different levels of a hierarchy. Sharma's CDFGs and expression trees, by contrast, are flowcharts that illustrate functions of the HDL code from which they are derived. Unlike Applicants' two-dimensional schematic representations, Sharma's expression trees in FIG. 5a and 5b are not a hierarchical diagram that contains all state elements and combinatorial logic that can be abstracted at different levels of a hierarchy. Thus, Sharma does not teach a two-dimensional schematic representation that includes a set of Register Transfer Diagrams.

Unlike Sharma's CDFGs and expression trees, Applicants' two-dimensional schematic representations of an IC are not necessarily derived from pre-existing HDL. In other words, Applicants' schematic representations may be used to produce a circuit independently from the HDL. Thus, a designer could use either HDL, two-dimensional schematic representations, or a combination thereof to represent a circuit design.

As seen in FIG. 5a-5b, Sharma generates two dimensional diagrams; however, his diagrams are derived from the HDL and thus could not be generated independently from HDL.

Even if Sharma were to generate the CDFG or the expression tree independently from an HDL description, Sharma neither describes nor suggests embedding the HDL description within the CDFG or within the expression tree to produce a unified representation. Thus, Sharma does not teach embedding a computer instruction within a two-dimensional schematic representation of the logic design.

As described in Applicants' specification on pages 4-5, declarations and sensitivity lists are avoided to eliminate unnecessary updates. As such, Applicants' claim 1 clearly recites that the computer instruction is devoid of declarations which is neither disclosed or suggested by Sharma.

As seen in Sharma FIG. 4, that illustrates an example of HDL used in Sharma's invention, the HDL of element 68 contains a declaration. The portion of the code, *entity design is*, constitutes an entity declaration that assigns a specific name, in this case *design*, to the entity. Furthermore, in col. 11, lines 7 -11, another entity declaration is shown, *entity ic is*, along with a sensitivity list containing the entry, *clk*, in col. 11, line 13. Thus, Sharma does not teach a computer instruction being devoid of declarations or entries to a sensitivity list.

For at least the foregoing reasons, claim 1 is patentable over the reference. The limitations of claims 11 and 21 are similar to the limitations of claim 1 and thus claims 11 and 21 are patentable.

With respect to the rejection of Claims 7, 8, 10, 17, 18, 20, 27, 28, and 30 as being obvious over Sharma in view of the Jain Paper entitled A Comprehensive Pre-RTL IC Design Methodology, Applicants submit that the base reference Sharma neither describes nor suggests the features of the independent claims and Jain does not cure these deficiencies. Jain and Sharma's methods are based on flowchart representations of behavioral design descriptions while the Applicants' method includes a schematic representation of a structural design description.

The Examiner also takes the position that Jain's teachings of CDFGs being generated to alternate levels of design abstraction is common and well known in the art.

Applicants maintain that Sharma's and Jain's CDFGs are behavioral representations not schematic representations as claimed by Applicants in base claim 1. As such, generating CDFGs to alternate levels of behavioral design abstraction in Sharma and Jain has no bearing upon the schematic representation recited in claim 1. Accordingly, Jain adds nothing to Sharma with respect to Applicants' two-dimensional schematic representation or to abstracting alternate levels thereof.

Moreover, the combination of Jain and Sharma would not enable one skilled in the art to arrive at Applicant's claim 1. Specifically, because Jain like Sharma is directed to behavioral design representations. Neither of the references suggests generating a logic design that comprises embedding a computer instruction within a two-dimensional schematic representation of the logic design for use in designing an integrated circuit, the computer instruction being devoid of declarations and where the two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD). Thus, Applicant's dependent claims are allowable at least for the reasons discussed above and also define patentable features over the art.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claims, except as specifically stated in this paper, and the amendment of any claims does not necessarily signify concession of unpatentability of the claim prior to its amendment.

The prior art cited but not applied by the Examiner is seen as neither describing nor suggesting Applicants' invention whether taken separately or in combination with the art applied.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested.

Please apply any fees or credits due in this case to Deposit Account 06-1050, referencing Attorney Docket No. 10559-595001.

Respectfully submitted,

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Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

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